REMARKS

Claims 1-7 and 51-74 remain in the application. Reconsideration of the application in view of the amendments and the remarks to follow is requested.

Claims 1-7 and 51-73 stand rejected under 35 U.S.C. §102(e) as being anticipated by Forbes, U.S. Patent No. 5,897,351. The Examiner also asserts (p. 11, item 4) that "Claims stand rejected under 35 U.S.C. §103(a) as being unpatentable over Forbes, U.S. Patent No. 5,897,351." Applicants infer that the Examiner had intended to reject claims 52, 53 and 74. Clarification of the rejection is requested.

Anticipation is a legal term of art. In order to present a valid finding of anticipation, a number of different legal standards must be simultaneously satisfied: (i) the reference must include every element of the claim within the four corners of the reference (see MPEP §2121); (ii) the elements must be set forth as they are recited in the claim; (iii) the teachings of the reference cannot be modified (see MPEP §706.02, stating that "No question of obviousness is present" in conjunction with anticipation); and (iv) the reference must enable the invention as recited in the claim (see MPEP §2121.01).

The §102 rejection of claims 1-7 and 51-73 is believed to be in error. Specifically, the PTO and Federal Circuit provide that §102 anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). The corollary of this rule is that the absence from a cited §102 reference of any claimed element negates the anticipation. *Kloster*

Speedsteel AB, et al. v. Crucible, Inc., et al., 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986).

To further delineate and clarify the legal meaning of the term "anticipation", Applicants note the requirements of MPEP §2131, which states that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM." This MPEP section further states that "'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

Additionally, the reference must enable the claimed invention. This is explained in MPEP §2121.01, entitled "Use of Prior Art in Rejections Where Operability Is In Question". This MPEP section states that "In determining that quantum of prior art disclosure which is necessary to declare an applicant's invention 'not novel' or 'anticipated' within section 102, the stated test is whether a reference contains an 'enabling disclosure'... ." *In re Hoeksema*, 399 F.2d 269, 158 USPQ 596 (CCPA 1968). A reference contains an "enabling disclosure" if the public was in possession of the claimed invention before the date of invention. Forbes '351 does not enable

the invention as recited in the claims because Forbes '351 does not even describe it!

The Examiner states (p. 2) that Forbes '351 teaches "forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being no greater than 1 um, at least two being different (Fig.3 and Col.7, lines: 55-63)." The Examiner is mistaken on multiple grounds.

First, Fig. 3 shows a single active area ridge having a single width. Thus, Fig. 3 cannot possibly show a plurality of active areas, as recited in all of Applicant's independent claims.

Second, the passage appearing at col. 7, lines 55-63 is unrelated to Fig. 3. This passage describes Fig. 4F (see col. 7, line 58, and is reproduced below for the Examiner's convenience).

> Active areas which define the silicon island-like active areas 300 are then defined on the individual silicon bars 404, using a standard process, such as LOCal Oxidation of Silicon (LOCOS), as shown in **FIG. 4F**, to form oxide 416 between the active areas 300. Depending on the width of the silicon bars 404, the area of these active areas 300 is approximately one square micron or less for sub-micron technology and approximately 0.0625 square microns or less for sub-0.25 micron technology.

This is clearly and plainly a reference that is discussing multiple wafers, each incorporating different respective characteristic linewidths. In other words, the reference relied upon by the Examiner (on p. 2, and also on p. 3, first full paragraph) does not describe plural active areas of more than one size on one substrate, and Forbes '351 makes no representation to that effect.

Put another way, the Examiner's mis-statement (p. 3, first full ¶) that "Col.7, lines60-61 states "these active areas 300 is approximately one square micron or less" is incorrect. Forbes is teaching a process that may be used in one instance to produce a wafer having a first set of active areas, all of the same first size, and another, different wafer having a second set of active areas, all the same second size.

This can be independently corroborated, for example, by looking at Figs. 4A through 4I. Note that these areas are explicitly depicted as being the same. In other words, using simple measurement tools, the Examiner can see that the interpretation of Forbes '351 supplied in this Action and other Actions is without support in the reference. In other words, the Examiner's interpretation of the teachings of the reference is inconsistent with the teachings of the reference.

There is no representation anywhere in Forbes '351 regarding multiple active areas having different widths that are formed on a common substrate, as recited in each of Applicant's independent claims.

Third, Figs. 4A through 4F unambiguously show that the silicon bars 404 formed on any individual substrate have a single common width, in direct and stark contrast to the invention as recited in claim 1 ("forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different"), claim 54 ("forming a plurality of shallow trench isolation regions received within a

substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths over the substrate, at least two of the widths being different, at least one of the plurality of active areas having a width less than one micron") or claim 63 ("forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different").

In other words, each of Applicant's independent claims clearly and unambiguously recite that multiple active widths are formed on a substrate. Forbes '351 fails to teach or disclose any such thing.

Fourth, Forbes '351 does not teach shallow trench isolation. In fact, Forbes '351 is void of the word "shallow". In other words, the term "shallow" does not appear anywhere in Forbes '351.

Fifth, Forbes '351 teaches use of LOCOS techniques for isolation. See, e.g., col. 7, lines 55-63. Forbes '351 also teaches methods described at col. 6, line 30 through col. 8, line 37 to form silicon bars 404. Forbes also teaches that these may be formed using processes as described at col. 6, lines 47-62. These techniques are not shallow trench isolation, and Forbes certainly does not represent them as such.

Sixth, the terms "LOCOS" and "shallow trench isolation" are terms of art having specific and different meanings to those of ordinary skill in the semiconductor arts. Copies of pp. 330-1 and 367-8, taken from S. Wolf, "Silicon Processing for the VLSI Era", copyright 1995, Lattice Press, Sunset

Beach, CA, describing these two, different technologies, have been provided for the Examiner's convenience. Note in particular that the text on p. 367 contrasts these two technologies and further shows why these two technologies are not arbitrarily interchangeable. The definition of the term "shallow trench isolation" provided in Wolf also makes clear that the methods for isolation of silicon islands taught by Forbes '351 are not arbitrarily interchangeable with shallow trench isolation as recited in all of Applicant's independent claims.

The Examiner states (p. 4) that "However, Examiner is not clear as to why applicant presents such lengthy arguments, since we both agree that LOCOS and STI are not the same."

Applicants will attempt to lay this out for the Examiner in a nutshell.

1) Forbes '351 teaches use of LOCOS techniques.

2) Forbes '351 is being cited as anticipating Applicant's claims.

3) Applicant's claims do not recite LOCOS.

4) Applicant's claims recite STI.

5) Forbes '351 does not teach or disclose STI.

6) Anticipation requires that the reference teach or disclose the claimed subject matter.

7) Therefore, Forbes '351 does not anticipate the invention as recited in any of Applicant's claims.

8) As a result, the anticipation rejections are in error and should be withdrawn, and Applicant's claims 1-7 and 51-73 should be allowed.

Seventh, it is inappropriate to modify the teachings of a reference in attempting to make a valid anticipation rejection under 35 U.S.C. §102. This is explained more fully in MPEP §706.02.

In a subsection entitled "DISTINCTION BETWEEN 35 U.S.C. 102 AND 103", this MPEP section states that: "The distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No question of obviousness is present." In other words, no modification or inference is allowed in a determination of anticipation. Put another way, the identical invention must be described and enabled within the four corners of the reference to provide a valid finding of anticipation.

Forbes '351 simply does not describe the invention as recited in any of Applicant's claims. It is not appropriate to modify the teachings of Forbes '351 to try to find anticipation.

Eighth, substituting the silicon bar structures 404 taught by Forbes '351 for the shallow trench isolation structures recited in all of Applicant's independent claims gives the term "shallow trench isolation" a meaning repugnant to the normal meaning of the term.

Applicant notes the requirements of MPEP §608.01(o), entitled "Basis for Claim Terminology in Description". This MPEP section states that "The meaning of every term used in any of the claims should be apparent from the descriptive portion of the specification with clear disclosure as to its import; and in mechanical cases, it should be identified in the descriptive portion of the specification by reference to the drawing, designating the part or parts

therein to which the term applies. A term used in the claims may be given a special meaning in the description. No term may be given a meaning repugnant to the usual meaning of the term.

The Examiner's arbitrary conflation of terms of art, including LOCOS, shallow trench isolation and deep trenches gives each of these terms meanings repugnant to the usual meanings of these terms as used by those of ordinary skill in the art. Such is improper and should be retracted.

The Examiner states (p. 4) that "Applicant argues that Forbes teaches LOCOS isolation rather than trench isolation and refers to Col.7, Lines: 55-63 as teaching that LOCOS isolates the active region. Examiner has reviewed the entire Forbes reference and cannot find where LOCOS is used to isolate the active region." An example of such teaching is found at col. 7, lines 55-63 and is reproduced below for the Examiner's aid in understanding what the reference the Examiner has chosen to cite in fact recites:

> Active areas which define the silicon island-like active areas 300 are then defined on the individual silicon bars 404, using a standard process, such as LOCal Oxidation of Silicon (**LOCOS**), as shown in FIG. 4F, to form oxide 416 between the active areas 300. Depending on the width of the silicon bars 404, the area of these active areas 300 is approximately one square micron or less for sub-micron technology and approximately 0.0625 square microns or less for sub-0.25 micron technology.

Forbes fails to describe such as shallow trench isolation (or "STI"). Wolfe points out clearly (§6.5, p. 367) that STI involves a number of steps, including oxide refill followed by planarization. Oxide refill is typically carried out by thermal decomposition of tetraethylorthosilicate ("TEOS"), for various

technical reasons. A principal such reason is that this can be accomplished without the lateral encroachment engendered by, for example, LOCOS, which encroachment is clearly shown in Forbes '351 (compare Figs. 4C and 4D).

As noted above, the term of art "shallow trench isolation" refers to more than just a trench depth. Forbes does not use this language and does not describe such processes.

The Examiner makes a series of statements (p. 5) to the effect that Forbes teaches trench isolation, and attempts to re-characterize a number of statements made by the Examiner and Applicants. Forbes '351 does indeed teach trench isolation. Forbes '351 does not teach "shallow trench isolation", and Forbes '351 makes no such representation.

Additionally, such gives the term of art "shallow trench isolation" a meaning repugnant to the ordinary meaning of the term as used in the art and as evidence by Wolf.

Applicants note in passing that a very brief search on the USPTO patent database, limited to just the last four years, provides no less than 2,259 issued patents in which the words "shallow trench isolation" appear. This is credible evidence that these words are a term of art having a specialized meaning in the art.

The Examiner correctly notes that Forbes '351 uses the phrase "isolation trench" in the Abstract. Forbes '351 also points out (col. 7, line 55 et seq.) that LOCOS isolates active areas 300. This combination of isolation techniques is not shallow trench isolation. This is why Forbes '351 does not call it such.

Again, note that Forbes '351 DOES NOT USE this term. Using the PTO database, we find that Dr. Leonard Forbes is listed as an inventor on 155 issued patents. As such, the use of terminology employed in the '351 patent document is deliberate - it is not an oversight that the '351 document does not refer to "shallow trench isolation".

Ninth, arbitrarily substituting the processes taught by Forbes '351 for the shallow trench isolation recited in Applicant's independent claims requires modification of the teachings of the reference. It is inappropriate to modify the teachings of a reference in attempting to find anticipation.

Tenth, Forbes '352 fails to show, teach, describe or discuss transistors having different channel widths, as erroneously alleged in the Office Action. Channel width refers to the effective separation between the source and the drain of a transistor, and corresponds roughly to source-drain separation and acts as an upper bound for gate length. Figs. 4A through 4I and 6 each show a plurality of active areas formed on a substrate and all having identical widths.

The illustration of Forbes' Fig. 3 depicts a p-channel transistor and an n-channel transistor that are illustrated as having identical dimensions for both gate width and gate length. The use of merged p- and n-channel transistors by Forbes '351 is described at least in the Title, Field of the Invention, col. 2, lines 26-33; col. 3, lines 6-16; col. 4, lines 29-32 and 61-65; col. 6, lines 7-9 etc. Forbes '351 is silent with respect to multiple channel or active area widths on a single substrate and thus cannot possibly teach or disclose the invention as recited in any of Applicant's claims.

The Examiner states (p. 6) that "FORBES DOES TEACH shallow trench isolation", based on the ordinary meanings of the terms "shallow", "trench" and "isolation". As used in the electrical arts, the term of art "shallow trench isolation" does not simply mean "a shallow trench that isolates". It refers to a much more specific process, and Applicants have provided credible, objective evidence to this effect.

The Examiner also states (p. 6) that "Forbes teaches the exact same process of forming and refilling the trenches with an oxide - Col.7, lines:48-56 describes refilling the shallow trenches." The Examiner is again mistaken.

Applicants reproduce that text below, along with the text immediately preceding it (col. 7, lines 20-56):

> The substrate 301 is oxidized using a standard silicon processing furnace at a temperature of approximately 900 to 1,100 degrees Celsius, followed by stripping of the Si_3N_4 cap 406, producing the structure shown in FIGS. 4D and 4E. A wet, oxidizing ambient is used in the furnace chamber to oxidize the exposed silicon regions on the lower part of the trenches 402 in a parallel direction to the surface of the substrate 301. The substrate 301 is oxidized for a time period, such that oxide 302 partially undercuts the bottom of the silicon bars 404, producing first portions of the silicon bars from which the island-like active areas 300 of silicon material will be defined in a subsequent process step, which are partially isolated from the substrate by the layer of oxide 302, and second portions of the silicon bars that define the pedestals 304 which support the silicon islands 300 that will be formed and which remain in contact with the substrate. In contrast to the process disclosed in the referenced patent application, in the process according to the present invention, the island-like active areas of silicon subsequently produced are not completely isolated from the substrate 301 by oxidation. A portion of the pedestal 304 is maintained to contact the body of the n-channel transistor 28 and a portion 304a of the pedestal is maintained to be in contact with the drain region 49 of the p-channel transistor 26 that is formed in a subsequent process step, the pedestal portion 304a being shown in FIG. 3 in contact with the drain region 49.

> The larger volume of oxide substantially fills the trenches 402 between the silicon bars 404. The time period for oxidation depends on the width of the silicon bars 404 and the effective width after the undercut step. For example, for sub-micron technology, oxidation time is approximately three to four hours. For sub-0.25 micron technology, oxidation time is approximately one hour.

Forbes '351 is using a Si_3N_4 cap to **LOC**ally **O**xidize **S**ilicon to provide oxide 302. The Si_3N_4 cap prevents some silicon from reacting with oxygen, while exposed silicon is locally oxidized. Forbes '351 is not teaching STI in the conventional sense of the term. In other words, the resemblance that the Examiner is noticing to STI in the teachings of Forbes '351 is superficial and is based on a misunderstanding of the meaning of the term "shallow trench isolation" as it is used by those of ordinary skill in the relevant arts.

Applicants have provided the Examiner with technical information describing both techniques. LOCOS, once again, is an acronym derived from LOcal Oxidation of Silicon, with the underlined and capitalized letters forming the acronym. This technique has nothing to do with deposition of oxide. LOCOS uses a deep oxidation of the silicon substrate itself to provide what is known in the art as a Field OXide or "FOX". No trenches are formed or involved in LOCOS.

Shallow trench isolation techniques, on the other hand, involve formation of a vertical-walled trench, typically using reactive ion etching, followed by deposition of silicon dioxide, rather than oxidation of the silicon substrate material. As a result, shallow trench isolation features can be formed with far more control over lateral spread that occurs due to diffusion

of oxygen in the oxide as it forms when the substrate itself is oxidized. This permits much greater packing density to be achieved. It also provides a more planar surface because the excess deposited oxide is removed using chemical-mechanical planarization techniques.

Applicants claim such a process in conjunction with other aspects of the invention. As noted above and in the last response, these techniques are not arbitrarily interchangeable.

Applicant is simply pointing out that Forbes '351 does not teach any form of shallow trench isolation, as recited in Applicant's claims and as understood by those of skill in the relevant arts, and instead teaches formation of isolation regions using a different conventional isolation technique known as LOCOS, albeit in an unusual form.

As a result, Forbes fails to teach or disclose, or provide enabling disclosure for, or suggest or motivate, the invention as recited in any of Applicant's claims. Since Forbes '351 fails to meet any of the criteria for anticipation, Forbes '351 cannot possibly meet them simultaneously.

Accordingly, and for at least these reasons, the anticipation and unpatentability rejections of claims 1-7 and 51-73 are clearly in error and should be withdrawn, and claims 1-7 and 51-73 should be allowed.

Dependent claims 2-7, 51-53, 55-62, 64-66 and 68-74 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

In view of the foregoing, allowance of claims 1-7 and 51-74 is requested. The Examiner is requested to phone the undersigned in the event

that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Apr. 3, 2002 By: _____

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Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Inventor .....Luan C. Tran
Assignee ..... Micron Technology, Inc.
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37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY
RESPONSE TO JANUARY 3, 2002 OFFICE ACTION
AMENDMENT TO ACCOMPANY CPA FILING

Deletions are bracketed, additions are underlined.

No amendments have been made to the claims, specification or drawings.

END OF DOCUMENT